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DESCRIPTION

INPUT CONTROL APPARATUS AND INPUT CONTROL METHOD

5   Technical Field

[0001]   The present invention relates to an input control
apparatus and input control method for quantizing data
used for decoding.

10   Background Art

[0002]   FIG.1 is a block diagram showing the configuration
of a conventional OFDM (Orthogonal Frequency Division
Multiplex) transmission apparatus 10 and OFDM reception
apparatus 20.   First,   the   configuration   of   OFDM
15   transmission   apparatus   10   will   be   explained.
Transmission data of a bit sequence is subjected to channel
coding (turbo coding) by coder 11, and the coded signal
is subjected to data iteration processing and puncturing
processing (rate matching processing) by rate matching
20   section 12.   The signal after the rate matching processing
is subjected to data modulation mapping by modulation
section 13 and output to IFFT (Inverse Fast Fourier
Transform) section 14.

[0003]   The signal output from modulation section 13 is
25   subjected to an inverse fast Fourier transform by IFFT
section 14, and an OFDM signal is thereby formed and a
guard interval is inserted into the OFDM signal by GI

(Guard Interval) insertion section 15. The OFDM signal with the guard interval inserted is converted from a digital signal to an analog signal by D/A conversion section 16, and the analog signal is up-converted to a radio frequency by RF (Radio Frequency) conversion section 17 and sent to OFDM reception apparatus 20 through antenna 18.

[0004] Next, the configuration of OFDM reception apparatus 20 will be explained. Noise is superimposed on the signal sent from OFDM transmission apparatus 10 over the propagation path and the signal is received by antenna 21. The signal received by antenna 21 is down-converted from a radio frequency to an intermediate frequency by RF conversion section 22, separated (subjected to quadrature detection) into signals of I component and Q component channels and then output to A/D conversion section 23. The signals of the I component and Q component channels are converted from analog to digital by A/D conversion section 23, and with guard intervals removed by GI removing section 24, the digital signals are output to FFT (Fast Fourier Transform) section 25.

[0005] The signals output from GI removing section 24 are separated into sequences in subcarrier units by FFT section 25 and the separated signals are demodulated by demodulation section 26. The demodulated signals are subjected to rate dematching processing by rate

demathing section 27 and the signals subjected to the rate dematching processing are separated into three sequences by separation section 28. The same number of bits are deleted from the three separated sequences by

5   bit number reduction section 29 and each sequence from which the bits have been deleted is subjected to channel decoding (turbo decoding) by decoder 30 and received data is thereby obtained.

[0006] FIG.2 is a block diagram showing the internal

10   configuration of coder 11 of OFDM transmission apparatus 10. In this figure, systematic bit sequence (transmission data) u is output as systematic bit sequence X1 as is, while it is also input to element coder 31 and interleaver 32. Element coder 31 generates a codeword

15   for input systematic bit sequence u. The generated codeword is output as parity bit sequence X2.

[0007] Interleaver 32 has a conversion function for converting a read order corresponding to a write order and outputs input systematic bit sequence u to element

20   coder 33 in a different order from the input order. Element coder 33 generates a codeword for the bit sequence output from interleaver 32. The generated codeword is output as parity bit sequence X3.

[0008] FIG.3 is a block diagram showing the internal

25   configuration of decoder 30 of OFDM reception apparatus 20. The received signal sequences have noise (assumed to be additive white Gaussian noise here) and correspond

to a systematic bit and a parity bit respectively. These
received signal sequences are input to decoder 30.

[0009] Element decoder 41 performs decoding processing
on the received signal sequence corresponding to
systematic bit sequence X1 (hereinafter referred to as
"systematic part Y1") and the received signal sequence
corresponding to parity bit sequence X2 (hereinafter
referred to as "parity part Y2") together with a priori
value La1 which is reliability information transmitted
from deinterleaver 45 and outputs external value Le1 to
interleaver 42. The external value indicates the
increase in symbol reliability by the element decoder.
External value Le1 is rearranged by interleaver 42 and
input to element decoder 44 as a priori value La2. Note
that decoding by element decoder 44 is not performed in
a first iteration, and therefore 0 is assigned as a priori
value.

[0010] Element decoder 44 receives a sequence obtained
by rearranging systematic part Y1 by interleaver 43, the
received signal sequence corresponding to parity bit
sequence X3 (hereinafter referred to as "parity part Y3")
and a priori value La2, performs decoding processing on
them and outputs external value Le2 to deinterleaver 45.
External value Le2 is subjected to an operation by
deinterleaver 45 of restoring the order before rearranged
by the interleaver, input to element decoder 41 as a priori
value La1 and decoded repeatedly. After being decoded

several or over ten times repeatedly, element decoder 44 calculates a posteriori value L2 defined as a logarithmic posterior probability ratio and deinterleaver 46 deinterleaves the calculation result.

5 Hard decision section 47 then performs hard decision on the deinterleaved sequence, outputs the decoded bit sequence, and error detection section 48 performs error detection on the decoded bit sequence and outputs the detection result.

10 Non-Patent Document 1: C. Berrou, A. Glavieux "Near Optimum Error Correcting Coding And Decoding: Turbo-Codes," IEEE Trans. Commun., Vol. 44, pp. 1261-1271, Oct. 1996.

15 Disclosure of Invention
Problems to be Solved by the Invention
[0011] However, the above described conventional turbo decoder has the following problems. The soft information bits of the systematic part and parity parts are quantized
20 uniformly without any distinction between the systematic part and parity parts, and therefore the number of bits input to the turbo decoder is fixed and the same number of bits of systematic part Y1, parity parts Y2 and Y3 are input to the turbo decoder. The circuit scale of the
25 turbo decoder largely depends on the memory capacity used for decoding calculations, and requires a memory capacity in accordance with the number of bits input to the turbo

decoder. Therefore, there is a problem that it is not possible to reduce the memory capacity or the circuit scale. The coding rate may be increased to reduce the memory capacity, but in such a case, data of the parity parts may be reduced and the error rate characteristic also deteriorates, and therefore the circuit scale cannot be reduced.

[0012] Furthermore, in the actual system, the coding rate and coding block length are variable, and therefore the system requires a minimum coding rate defined by the system and a memory capacity capable of responding to a longest block length, but all the memory capacity is not always used, which results in a problem that there remains a free space and memory is not used effectively.

[0013] It is therefore an object of the present invention to provide an input control apparatus and input control method that suppress characteristic deterioration, reduce the circuit scale of a turbo decoder and allow effective use of the memory of the turbo decoder.

Means for Solving the Problem

[0014] The input control apparatus of the present invention adopts a configuration having a bit number reduction section that reduces the number of bits of a systematic part and the number of bits of parity parts having a plurality of sequences input to a turbo decoder and a control section that controls the bit number

reduction section so that the number of bits of one sequence

of the parity parts falls below the number of bits of

the systematic part.

[0015]   According to this configuration, the number of

bits is reduced so that the number of bits of one sequence

of the parity parts input to the turbo decoder falls below

the number of bits of the systematic part, and it is thereby

possible to perform a decoding calculation of the turbo

decoder with a smaller number of bits and reduce the memory

capacity used for this calculation.

Advantageous Effect of the Invention

[0016]   With regard to the number of bits input to the

turbo decoder, the present invention can reduce the memory

capacity of the turbo decoder and thereby reduce the

circuit scale by reducing the number of bits of one sequence

of the parity parts compared to the number of bits of

the systematic part..Furthermore, the present invention

enables effective use of memory by changing the number

of bits of the systematic part and the number of bits

of the parity parts input to the turbo decoder in accordance

with a coding rate and/or coding block length.

Brief Description of Drawings

[0017]

    FIG.1 is a block diagram showing the configuration

of a conventional OFDM transmission apparatus and OFDM

reception apparatus;

FIG.2 is a block diagram showing the internal configuration of a coder of a conventional OFDM transmission apparatus;

5   FIG.3 is a block diagram showing the internal configuration of a decoder of a conventional OFDM reception apparatus;

FIG.4 is a block diagram showing the configuration of an OFDM reception apparatus according to Embodiment 10 1 of the present invention;

FIG.5 illustrates a bit number reduction section; and

FIG.6 illustrates a simulation result of the OFDM reception apparatus according to Embodiment 1 of the 15 present invention.

Best Mode for Carrying Out the Invention

[0018] Now, an embodiment of the present invention will be explained with reference to the attached drawings.
20 [0019]

(Embodiment 1)

FIG.4 is a block diagram showing the configuration of an OFDM reception apparatus according to Embodiment 1 of the present invention. In this figure, a signal 25 transmitted from a transmission apparatus is received by antenna 101 and output to RF (Radio Frequency) conversion section 102.

[0020]   RF conversion section 102 down-converts the frequency of a signal received by antenna 101 from a radio frequency to an intermediate frequency and separates it into signals of I component and Q component channels (quadrature detection).   The signals separated into the I component and Q component channels are output to A/D conversion section 103 respectively.

[0021]   A/D conversion section 103 converts the signal output from RF conversion section 102 from an analog signal to a digital signal and outputs the digital signal to GI (Guard Interval) removing section 104.

[0022]   GI removing section 104 deletes a guard interval from the signal output from A/D conversion section 103 and outputs the signal from which the guard interval has been deleted to FFT (Fast Fourier Transform) section 105.

[0023]   FFT section 105 applies a fast Fourier transform to the signal output from GI removing section 104 and separates the signal into sequences in subcarrier units. The separated signals are output to demodulation section 106.

[0024]   Demodulation section 106 demodulates the signal output from FFT section 105, and rate dematching section 107 performs rate dematching processing on the demodulated signal and outputs the signal to separation section 108.

[0025]   Separation section 108 separates the signal output from rate dematching section 107 into a sequence

of the received signal corresponding to a systematic bit
sequence (hereinafter referred to as "systematic part
Y1") and a sequence of the received signal corresponding
to a parity bit (hereinafter referred to as "parity part")

5   and outputs the respective separated sequences to bit
number reduction section 109. The parity parts are
separated into parity parts Y2 and Y3 corresponding to
parity bit sequences X2 and X3 respectively. Here,
suppose the separated sequences have the same number of

10 bits, which is K bits.

[0026] Bit number reduction section 109 reduces
respectively the number of bits of systematic part Y1
and parity parts Y2 and Y3 output from separation section
108 under the control of control section 110. Systematic

15 part Y1, and parity parts Y2 and Y3 with a reduced number
of bits are output to decoder 111. Suppose the number
of bits of systematic part Y1 output to decoder 111 is
M bits and the number of bits of parity parts Y2 and Y3
output to decoder 111 is L bits respectively.

20 [0027] Control section 110 acquires information on the
coding rate and coding block length of the received signal,
determines the number of bits of systematic part Y1, and
parity parts Y2 and Y3 in accordance with the coding rate
and/or coding block length so that the number of bits

25 L of one sequence of the parity parts falls below the
number of bits M of systematic part Y1, and controls bit
number reduction section 109 so that the determined number

of bits is obtained. More specifically, control section
110 performs control so that when the coding rate is low,
the number of bits L of the parity parts decreases and
when the coding rate is high, the number of bits L of
5   the parity parts increases. On the other hand, control
section 110 performs control such that when the coding
block length is short, the number of bits L of the parity
parts increases and when the coding block length is long,
the number of bits L of the parity parts decreases. This
10   makes it possible to reduce the range of variation in
the number of bits per block input to the turbo decoder,
thereby reducing the unused, free space of memory and
enabling effective use of memory.

[0028]   Decoder 111 performs channel decoding (turbo
15   decoding) on the signal output from bit number reduction
section 109 and obtains received data.

[0029]   Here, the method whereby control section 110
determines the number of bits input to decoder 111 will
be explained. Control section 110 has the following
20   general control equation:

$$M, L = f(R, N_{block}) \quad \dots \text{(Equation 1)}$$

M: Number of bits of systematic part Y1

L: Number of bits of parity parts Y2 and Y3

R: Coding rate

25   N_{block}: Coding block length

[0030]   In above Equation (1), if M is fixed and L is
expressed as a function of R, L can be expressed by the

following equation:

$$L = \text{int}\left[M \times \left(1 - \log_3 3R\right)\right] \quad \dots \text{(Equation 2)}$$

[0031] where, int is a maximum integer that does not exceed the value of the equation in parentheses. In Equation (2), if, for example, R=1, then L=0. In this equation, when coding rate R is low, the number of bits L of the parity parts increases and when the coding rate R is high, the number of bits L of the parity parts decreases.

[0032] Furthermore, M and L can be obtained using the following method. That is, when certain integer C is used, M can be expressed by following Equation (3) and L can be expressed by Equation (4):

$$M = \text{int}\left[C \times \frac{N_{max}}{N_{block}}\right] \quad \dots \text{(Equation 3)}$$

$$L = M - H \quad \dots \text{(Equation 4)}$$

[0033] where, N_{max} is a maximum coding block length. Furthermore, suppose H is an integer and satisfies 0<H<=M. In this Equation (3), M and L increase as N_{block} decreases and M and L decrease as N_{block} approximates to N_{max}. For example, when $N_{block}=N_{max}/2$, M=2×C, and L=M-H.

[0034] Thus, control section 110 determines the number of bits of systematic part Y1, and parity parts Y2 and Y3 input to decoder 111.

[0035] Next, bit number reduction section 109 will be explained more specifically. FIG.5 illustrates bit number reduction section 109. In this figure, suppose

the bit sequence of systematic part Y1 output from separation section 108 is 12 bits of "101110001110" and the bit sequence of parity part Y2 is 12 bits of "110010110111." Likewise, suppose the bit sequence of

5 parity part Y3 is 12 bits of "011001110001."

[0036] Bit number reduction section 109, controlled by control section 110, deletes bits of each input bit sequence so that systematic part Y1 is 6 bits, parity part Y2 is 4 bits and parity part Y3 is 4 bits. This causes

10 the bit sequence of systematic part Y1 output from bit number reduction section 109 to become "101110", the bit sequence of parity part Y2 to become "1100" and the bit sequence of parity part Y3 to become "0110."

[0037] Thus, in turbo decoding, bit number reduction

15 section 109 causes one sequence of the parity parts which have a lower degree of significance than that of the systematic part to have a smaller number of bits than the systematic part. This allows decoding calculation of the turbo decoder to be performed with a smaller number

20 of bits, thereby reducing the memory capacity. Note that bit number reduction section 109 deletes the lower bits and outputs the higher bits out of the input bits.

[0038] FIG.6 shows a simulation result of the OFDM reception apparatus according to Embodiment 1 of the

25 present invention. Here, the simulation specifications are as follows:

[0039]

Number of subcarriers: 1024

Spreading factor: 8

Modulation scheme (data): QPSK

Turbo block length: 3196

5   Channel coding: Turbo code (R=1/3, K=4) K: constraint

length, Max-Log-MAP decoding

Iteration count: 8

Channel model: AWGN

[0040]   In FIG.6, the vertical axis shows a BER (Bit Error

10   Rate) and the horizontal axis shows Eb/N0. Furthermore,

suppose the number of bits of the systematic part is 8

bits and the number of bits of the parity parts has three

patterns, namely 5, 6, and 8 bits. As is obvious from

this figure, the characteristics when the number of bits

15   of the parity part is 6 bits and 8 bits are completely

the same and even when the number of bits of the parity

part is 5 bits, deterioration is only approximately

0.05[dB] with a BER of 1.0E-04.   This is because the turbo

decoder performs iteration decoding and achieves a high

20   decoding characteristic. However, when the number of

bits of the parity parts is too small, it is also not

possible to realize a high decoding characteristic, and

therefore it is necessary to reduce the memory capacity

and avoid characteristic deterioration.

25   [0041] Thus, according to this embodiment, with regard

to the number of bits input to the turbo decoder, it is

possible to reduce the memory capacity of the turbo decoder

and thereby reduce the circuit scale by reducing the number of bits of one sequence of the parity parts compared to the number of bits of the systematic part. Furthermore, it is possible to effectively use memory by changing the number of bits of the systematic part and the number of bits of the parity parts input to the turbo decoder in accordance with the coding rate and/or coding block length.

[0042] This embodiment has explained the case where the turbo decoder is mounted on an OFDM reception apparatus as an example, but the present invention is not limited to this and is also applicable to cases where the turbo decoder is mounted on a reception apparatus using optical communication or a reproduction apparatus such as a magnetic disk and an optical disk. Furthermore, not only a turbo code but also a convolutional code can be used.

[0043] A first aspect of the present invention is an input control apparatus having a bit number reduction section that reduces the number of bits of a systematic part and the number of bits of parity parts having a plurality of sequences input to a turbo decoder and a control section that controls the bit number reduction section so that the number of bits of one sequence of the parity parts falls below the number of bits of the systematic part.

[0044] According to this configuration, by reducing the number of bits of the systematic part and the number of bits of the parity parts input to the turbo decoder so

that the number of bits of one sequence of the parity parts falls below the number of bits of the systematic part, it is possible to perform a decoding calculation of the turbo decoder with a smaller number of bits, thereby

5   reducing the memory capacity used for this calculation.

[0045] A second aspect of the present invention is the input control apparatus in the above described aspect, wherein the control section controls the bit number reduction section so that the number of bits of the parity

10   parts is obtained in accordance with a coding rate and/or coding block length of a bit sequence input to the turbo decoder.

[0046] According to this configuration, by reducing the number of bits of the systematic part and the number of

15   bits of the parity parts so that the number of bits of the parity parts is obtained in accordance with the coding rate and/or coding block length of the bit sequence input to the turbo decoder, it is possible to reduce the range of variation in the number of bits per block input to

20   the turbo decoder, thereby reducing unused, free space of memory and enabling effective use of memory.

[0047] A third aspect of the present invention is the input control apparatus in the above described aspect, wherein the control section performs control so that the

25   number of bits of the parity parts decreases as the coding rate of the bit sequence input to the turbo decoder decreases and the number of bits of the parity parts

increases as the coding rate increases.

[0048] According to this configuration, the number of bits of the parity parts decreases where the number of bits used for decoding increases as the coding rate decreases, the number of bits of the parity parts increases where the number of bits used for decoding decreases as the coding rate increases, and it is possible to thereby reduce the range of variation in the number of bits per block input to the turbo decoder, reduce unused free space of memory and effectively use memory.

[0049] A fourth aspect of the present invention is the input control apparatus of the above described aspect, wherein the control section performs control so that the number of bits of the parity parts decreases as the coding block length input to the turbo decoder increases and the number of bits of the parity parts increases as the coding block length decreases.

[0050] According to this configuration, the control section controls the bit number reduction section so that the number of bits of the parity parts decreases as the coding block length increases and the number of bits of the parity parts increases as the coding block length decreases, and it is possible to thereby reduce the range of variation in the number of bits per block input to the turbo decoder, reduce unused free space of memory and effectively use memory.

[0051] A fifth aspect of the present invention is an input

control method having the step of reducing the number
of bits of a systematic part and the number of bits of
parity parts so that the number of bits of one sequence
of the parity parts falls below the number of bits of

5   the systematic part out of the systematic part and parity
parts having a plurality of sequences input to a turbo
decoder.

[0052]   According to this method, by reducing the
respective numbers of bits in accordance with the coding

10   rate and/or coding block length of the bit sequence input
to the turbo decoder and so that the number of bits of
one sequence of the parity parts falls below the number
of bits of the systematic part, it is possible to reduce
the range of variation in the number of bits per block

15   input to the turbo decoder, thereby reducing unused free
space of memory and enabling effective use of memory.
Furthermore, it is possible to perform a decoding
calculation of the turbo decoder with a smaller number
of bits and thereby reduce the memory capacity used for

20   this calculation.

[0053]   The present application is based on Japanese
Patent Application No. 2003-333489 filed on September 25,
2003, entire content of which is expressly incorporated
by reference herein.

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Industrial Applicability

[0054]   With regard to the number of bits input to a turbo

decoder, the input control apparatus and input control method according to the present invention has the effect of reducing the memory capacity of the turbo decoder by reducing the number of bits of one sequence of parity

5   parts compared to the number of bits of a systematic part, and the effect of enabling effective use of memory by changing the number of bits of the systematic part and the number of bits of the parity parts input to the turbo decoder in accordance with a coding rate and/or coding

10   block length, and is suitable for use in an apparatus having a turbo decoder such as a reception apparatus using radio communication, reception apparatus using optical communication and reproduction apparatus such as a magnetic disk and optical disk.